Semiconductor manufacturing is the workhorse for a wide range of industries. Most semiconductor electronics are made from Silicon, and are fabricated using CMOS technology. The versatility of semiconductor electronics stems from the ever-reducing cost of integrating more computing and memory functions on chip. The small cost for adding extra functions has been maintained in the past 50 years through transistor scaling. Transistor scaling focuses on shrinking the size of transistors integrated on chip. This reduction in transistor size, while keeping the overall cost of the chip fixed allowed us to reduce the cost per function with scaling, and is what is celebrated as Moore’s law. Scaling has been working gracefully up to the last decade, where the exponential rise in manufacturing cost and diminishing gains of scaling on device performance reduce its economic benefit. To revive the cost reduction trend, different techniques were proposed such as augmenting CMOS manufacturing with new materials (Beyond CMOS), 3D integration, and integrating more non-transistor elements on-chip (More than Moore).

In this work, we focus on the efficient implementation of several circuit functions using an allotropy of carbon known as graphene. Despite its promising electronic properties, graphene circuits has been held back by a plethora of nonidealities and technological roadblocks that hamper its use in traditional transistor-based circuits. In this work, we attempt to leverage the unique physical properties of graphene to implement non von-Neumann neuromorphic computing architectures, low-loss diodes and evaluate the behavior of diffusive-transport graphene couplers. We focus on the the design, fabrication and characterization of graphene devices in the presence of the current performance-limiting technological nonidealities in heterogeneous graphene-CMOS systems. We present the design, fabrication and characterization of all-graphene resistive data converters devices and diodes, discussing their performance and application as building elements of all-graphene brain-inspired computing architectures. We evaluate the performance of graphene couplers operating in the diffusive transport regime, which serve as a method to analyze the cross-coupling between adjacent graphene interconnects. We also discuss the current technological limitations hampering the performance of graphene devices, and the roles of different processing non-idealities on the characteristics of graphene devices.